

UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Kedua
Sidang Akademik 1995/96

Mac/April 1996

ZSE 416 - Pengantar Mikropemprosesan/Mikrokomputer

Masa : [3 jam]

Sila pastikan bahawa kertas peperiksaan ini mengandungi TUJUH muka surat yang bercetak sebelum anda memulakan peperiksaan ini.

Jawab kesemua ENAM soalan. Kesemuanya wajib dijawab di dalam Bahasa Malaysia.

- 1(a) Tuliskan aturcara penghimpunan serta kod mesin (heksadesimal) bagi mengira $51 + 61 + 18 - 32$. Aturcara tersebut hendaklah disimpan di lokasi RAM bermula daripada alamat 2030H manakala jawapan daripada hasil pengiraan tersebut hendaklah disimpan di lokasi ingatan 20BBH. (40/100)
- (b) Nyatakan dua kegunaan utama stack. (20/100)
- (c) Rajah 1 menunjukkan kandungan semasa sebahagian ingatan dan alat daftar CPU yang sepadan. Tunjukkan kandungan bahagian ingatan dan alat daftar CPU tersebut selepas perlaksanaan turutan arahan berikut:

LDA FFEAH
ADC M
PUSH BC
PUSH DE
POP BC

Alamat Ingatan	Kandungan Ingatan	Bendera
FFEAH	0FH	0 0 1 0 0 0 1 1
FFEBH	F0H	Akumulator
FFECH	0FH	0FH
FFEDH	B4H	Alat Daftar BC
FFEEH	A7H	62H 17H
FFEFH	93H	Alat Daftar DE
FFF0H	14H	51H 33H
FFF1H	10H	Alat Daftar HL
FFF2H	21H	FFH EBH
FFF3H	72H	Penunjuk Stack
		FFH F0H

Rajah 1

(40/100)

- 2(a) Terangkan tiga jenis mod pengalamatan dan berikan satu contoh arahan bagi setiap mod pengalamatan tersebut.

(20/100)

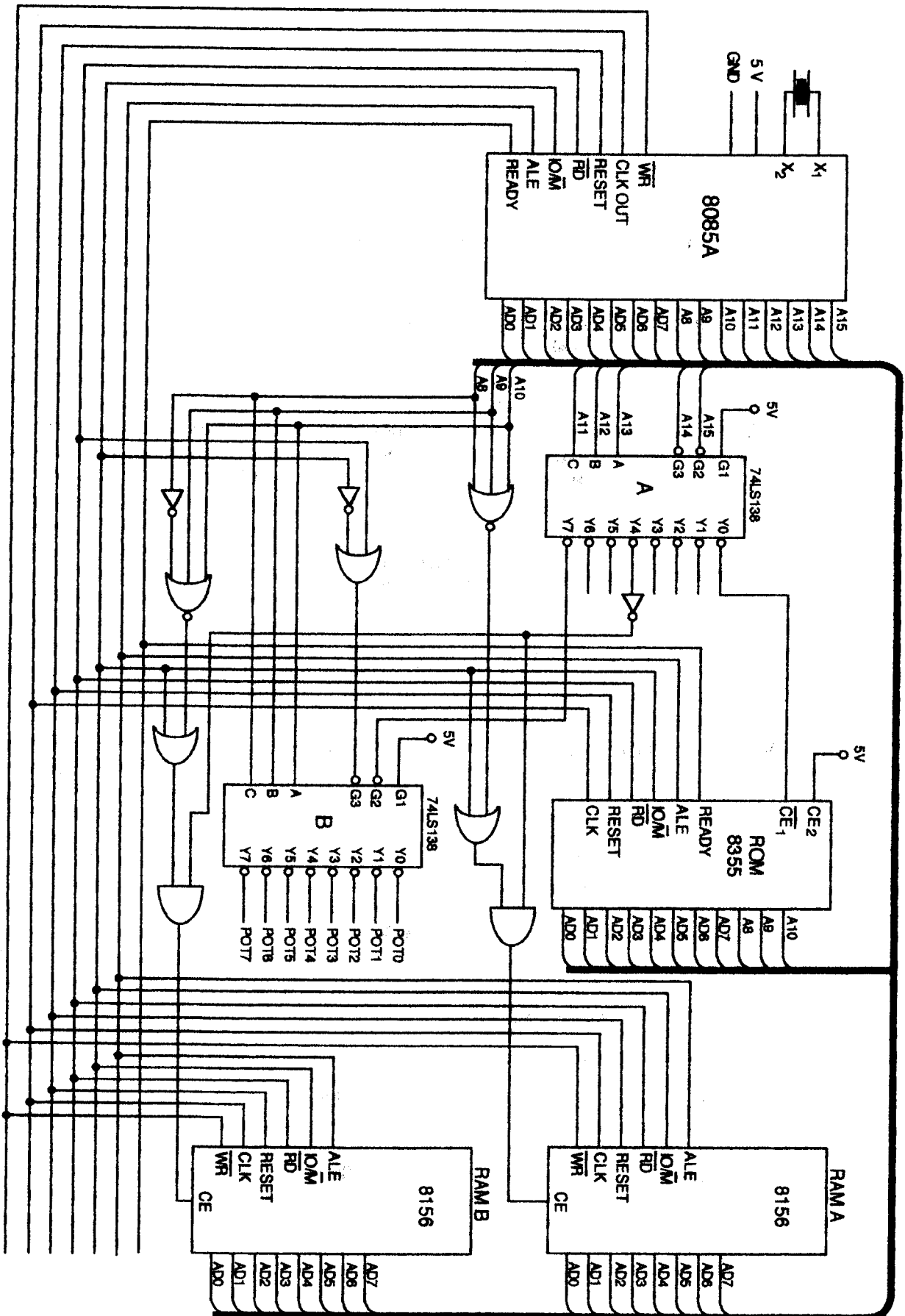
- (b) Fahami aturcara penghimpunan berikut:

MVI A, FEH
MVI B, 01H
MVI C, 32H

GELUNG: SUB B
DCR C
JNZ GELUNG
STA AAFH
HLT

Berdasarkan aturcara penghimpunan di atas:

- (i) Berapa kalikah DCR C dilaksanakan? (5/100)
 - (ii) Berapakah kalikah aturcara melompat ke GELUNG? (5/100)
 - (iii) Apakah kandungan ingatan AAFH setelah selesai aturcara di atas dilaksanakan? (5/100)
 - (iv) Kirakan masa yang diambil oleh sistem mikropemproses 8085 bagi melaksanakan aturcara tersebut sekiranya frekuensi jam adalah 2.5 MHz. (35/100)
 - (v) Bagaimanakah aturcara tersebut boleh diubahsuai supaya boleh melompat ke GELUNG sebanyak 250 kali? (15/100)
 - (vi) Bagaimana pula mengubahsuainya bagi melompat 300 kali? (15/100)
- 3(a) Terangkan maksud ingatan berlipat di dalam pengalamatan sesuatu sistem mikropemproses. (20/100)
- (b) Berdasarkan sistem mikropemproses 8085 dalam Rajah 2 tentukan alamat-alamat berikut:-
- (i) Lokasi alamat bagi ROM, RAM A dan RAM B (20/100)
 - (ii) Alamat bagi pot 0 hingga pot 7 (25/100)
 - (iii) Alamat-alamat lain yang dikodkan oleh pengekodan A (25/100)
 - (iv) Lokasi alamat yang tidak dikodkan oleh pengekodan A. (10/100)



Rajah 2

...5/-

- 4(a) Terangkan maksud *pertindihan ambil-laksana (fetch-execute overlap)* di dalam perlaksanaan arahan mikropemproses 8085.

(20/100)

- (b) Aturcara berikut di bawah merupakan aturcara ujian bagi memaparkan kitaran mesin di layar osiloskop. Fungsi keseluruhan aturcara tersebut ialah untuk mengambil data dari pot input 29H yang bernilai F0H, kemudian menyimpan data tersebut ke satu lokasi ingatan RAM.

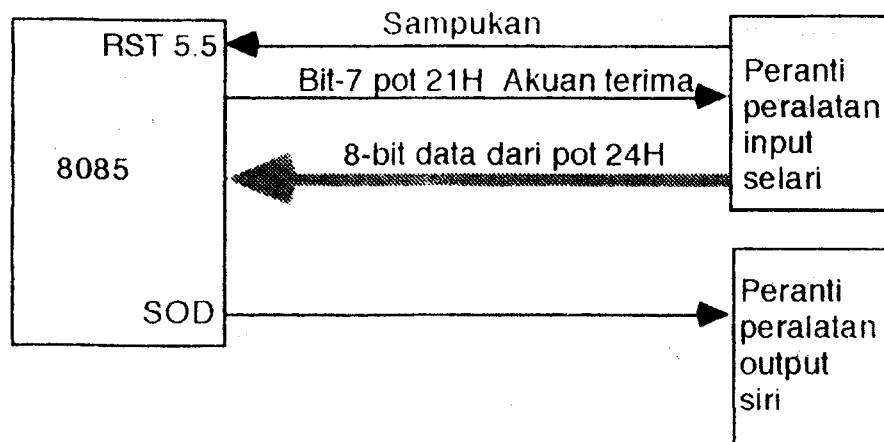
alamat	mnemonik	arahan
2010H	21H 30H 20H	LX1 H, 2030H
2013H	D8H 29H	GELUNG: IN 29H
2015H	77H	MOV M, A
2016H	C3H 13H 20H	JMP GELUNG
2019H	76H	HLT

- (i) Nyatakan lokasi RAM di mana data input tersebut disimpan. (10/100)
- (ii) Senaraikan pin-keluaran mikropemproses yang harus disambung kepada pemacu-luar osiloskop bagi memastikan arahan tersebut dilaksanakan oleh mikropemproses. (15/100)
- (iii) Terangkan bahagian manakah daripada aturcara tersebut di atas yang akan menghasilkan gelombang pegun di layar osiloskop? (10/100)
- (iv) Dengan menggunakan kertas gelombang isyarat yang dibekalkan, lukiskan gelombang pegun yang terhasil di layar osiloskop semasa aturcara tersebut dijalankan (run). Tuliskan nilai pada bus data dan alamat di setiap kitaran mesin dalam lakaran tersebut. (45/100)

- 5(a) Terangkan maksud ungkapan berikut merujuk kepada sampukan mikropemproses 8085:

- (i) Restart perisian (10/100)
- (ii) Restart perkakasan (10/100)
- (iii) Sampukan bertopeng (10/100)

- (b) Rajah 3 menunjukkan peranti peralatan yang disambung kepada sampukan RST 5.5. Selepas CPU menerima byte data daripada pot 24H, isyarat akuan terima akan dihantar semula kepada peranti peralatan melalui bit-7 pot 21 yang berlogik 1. Arahan di lokasi vektor RST 5.5 adalah JMP F100H.

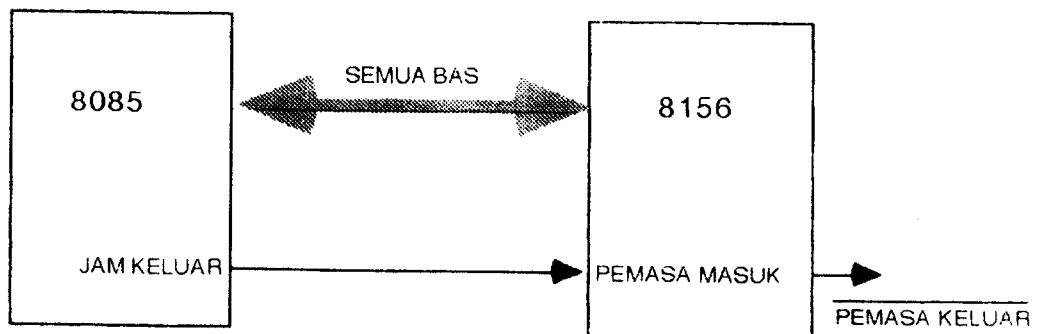


Rajah 3

- (i) Terangkan tindakbalas mikropemproses apabila ia menerima bit 1 daripada input RST 5.5 (30/100)
- (ii) Tunjukkan subrutin yang akan membaca data input daripada peranti peralatan tersebut kemudian mengeluarkannya secara selari melalui pin SOD. (40/100)
6. Suatu sistem mikropemproses 8085 menggunakan cip 8156 sebagai sebahagian daripada RAM dan pot input/output.
- (a) Sekiranya lokasi alamat RAM 8156 adalah 3000H hingga 30FFH tentukan alamat bagi:
- (i) Alat daftar status-perintah (5/100)
- (ii) Pot-pot input/output (10/100)
- (iii) Byte-byte pembilang pemas (5/100)

- 7 -

- (b) Rajah 4 menunjukkan pin jam keluaran mikropemproses 8085 disambung kepada input pemasa cip 8156. Sekiranya frekuensi jam adalah 2.5 MHz, tunjukkan segmen aturcara yang membolehkan pemasa keluaran cip 8156 mengeluarkan gelombang persegi 1 kHz secara berterusan, berserta dengan perintah pemula pemasa, membenarkan pot sampukan, menjadikan pot A sebagai pot input, pot B sebagai pot output dan pot C sebagai pot berjabat tangan sepenuhnya.



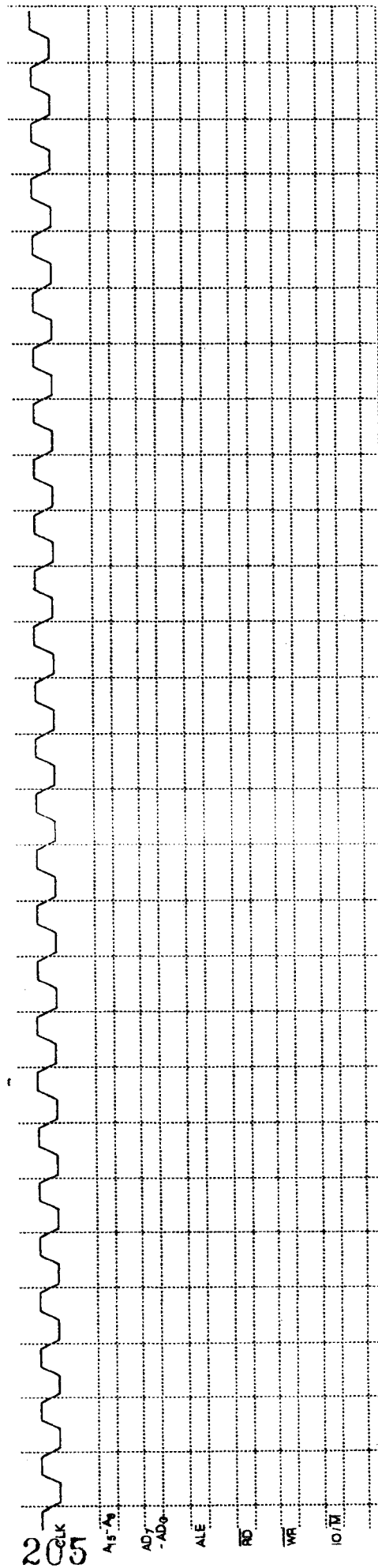
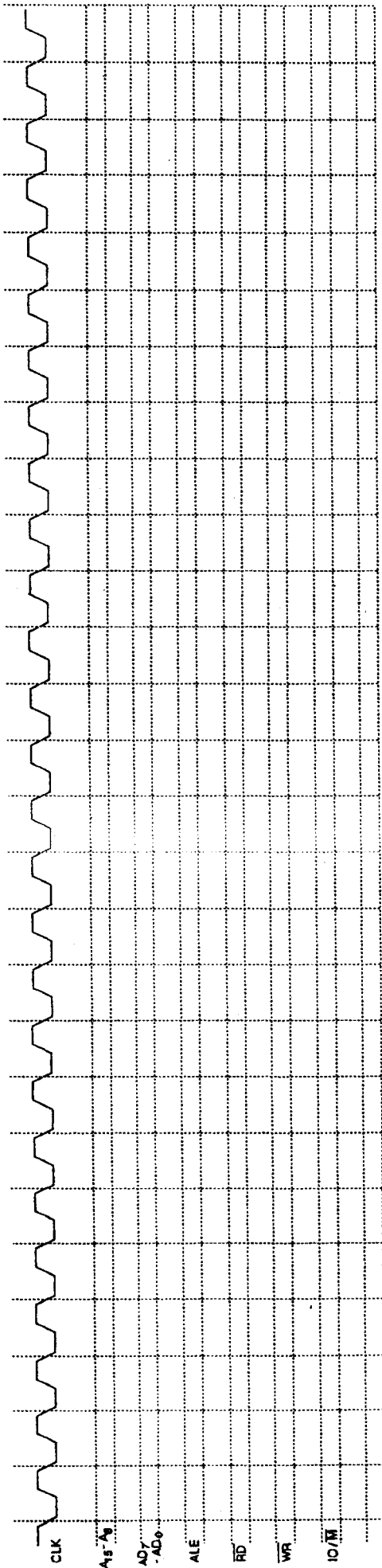
Rajah 4

(50/100)

- (c) Berdasarkan segmen aturcara (b) lukiskan litar pandu-sampuk yang berjabat tangan dengan pot A dan B.

(30/100)

- 0000000 -



8085 Instruction Set

4.6 INSTRUCTION SET ENCYCLOPEDIA

In the ensuing dozen pages, the complete 8085A instruction set is described, grouped in order under five different functional headings, as follows:

1. **Data Transfer Group** — Moves data between registers or between memory locations and registers. Includes moves, loads, stores, and exchanges. (See below.)
2. **Arithmetic Group** — Adds, subtracts, increments, or decrements data in registers or memory. (See page 4-13.)
3. **Logic Group** — ANDs, ORs, XORs, compares, rotates, or complements data in registers or between memory and a register. (See page 4-16.)
4. **Branch Group** — Initiates conditional or unconditional jumps, calls, returns, and restarts. (See page 4-20.)
5. **Stack, I/O, and Machine Control Group** — Includes instructions for maintaining the stack, reading from input ports, writing to output ports, setting and reading interrupt masks, and setting and clearing flags. (See page 4-22.)

The formats described in the encyclopedia reflect the assembly language processed by Intel-supplied assembler, used with the Intel development systems.

4.6.1 Data Transfer Group

This group of instructions transfers data to and from registers and memory. **Condition flags are not affected by any instruction in this group.**

MOV r1, r2 (Move Register)

(r1) — (r2)

The content of register r2 is moved to register r1.

0	1	D	D	D	S	S	S
---	---	---	---	---	---	---	---

Cycles: 1
States: 4
Addressing: register
Flags: none

MOV r, M (Move from memory)

(r) — ((H) (L))

The content of the memory location, whose address is in registers H and L, is moved to register r.

0	1	D	D	D	1	1	0
---	---	---	---	---	---	---	---

Cycles: 2
States: 7
Addressing: reg. indirect
Flags: none

MOV M, r (Move to memory)

((H) (L)) — (r)

The content of register r is moved to the memory location whose address is in registers H and L.

0	1	1	1	0	S	S	S
---	---	---	---	---	---	---	---

Cycles: 2
States: 7
Addressing: reg. indirect
Flags: none

MVI r, data (Move Immediate)

(r) — (byte 2)

The content of byte 2 of the instruction is moved to register r.

0	0	D	D	D	1	1	0
data							

Cycles: 2
States: 7
Addressing: immediate
Flags: none

MVI M, data (Move to memory immediate)

((H) (L)) — (byte 2)

The content of byte 2 of the instruction is moved to the memory location whose address is in registers H and L.

0	0	1	1	0	1	1	0
data							

Cycles: 3
States: 10
Addressing: immed./reg. indirect
Flags: none

LXI rp, data 16 (Load register pair immediate)

(rh) — (byte 3).

(rl) — (byte 2)

Byte 3 of the instruction is moved into the high-order register (rh) of the register pair rp. Byte 2 of the instruction is moved into the low-order register (rl) of the register pair rp.

0	0	R	P	0	0	0	1
low-order data							
high-order data							

Cycles: 3
States: 10
Addressing: immediate
Flags: none

LDA addr (Load Accumulator direct)

(A) — ((byte 3)(byte 2))

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register A.

0	0	1	1	1	0	1	0
low-order addr							
high-order addr							

Cycles: 4
States: 13
Addressing: direct
Flags: none

STA addr (Store Accumulator direct)

((byte 3)(byte 2)) — (A)

The content of the accumulator is moved to the memory location whose address is specified in byte 2 and byte 3 of the instruction.

0	0	1	1	0	0	1	0
low-order addr							
high-order addr							

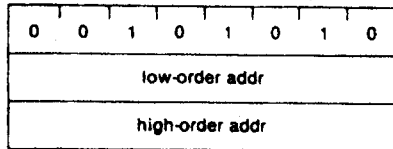
Cycles: 4
States: 13
Addressing: direct
Flags: none

LHLD addr (Load H and L direct)

(L) ← ((byte 3)(byte 2))

(H) ← ((byte 3)(byte 2) + 1)

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register L. The content of the memory location at the succeeding address is moved to register H.



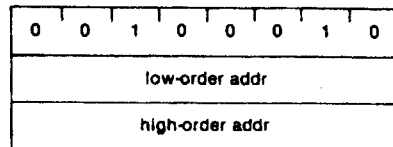
Cycles: 5
States: 16
Addressing: direct
Flags: none

SHLD addr (Store H and L direct)

((byte 3)(byte 2)) ← (L)

((byte 3)(byte 2) + 1) ← (H)

The content of register L is moved to the memory location whose address is specified in byte 2 and byte 3. The content of register H is moved to the succeeding memory location.

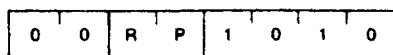


Cycles: 5
States: 16
Addressing: direct
Flags: none

LDAX rp (Load accumulator indirect)

(A) ← ((rp))

The content of the memory location, whose address is in the register pair rp, is moved to register A. Note: only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.

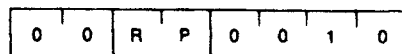


Cycles: 2
States: 7
Addressing: reg. indirect
Flags: none

STAX rp (Store accumulator indirect)

((rp)) ← (A)

The content of register A is moved to the memory location whose address is in the register pair rp. Note: only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.



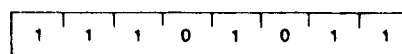
Cycles: 2
States: 7
Addressing: reg. indirect
Flags: none

XCHG (Exchange H and L with D and E)

(H) ← (D)

(L) ← (E)

The contents of registers H and L are exchanged with the contents of registers D and E.



Cycles: 1
States: 4
Addressing: register
Flags: none

4.6.2 Arithmetic Group

This group of instructions performs arithmetic operations on data in registers and memory.

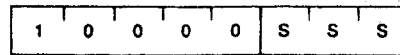
Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Carry, and Auxiliary Carry flags according to the standard rules.

All subtraction operations are performed via two's complement arithmetic and set the carry flag to one to indicate a borrow and clear it to indicate no borrow.

ADD r (Add Register)

(A) ← (A) + (r)

The content of register r is added to the content of the accumulator. The result is placed in the accumulator.

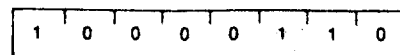


Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ADD M (Add memory)

(A) ← (A) + ((H)(L))

The content of the memory location whose address is contained in the H and L registers is added to the content of the accumulator. The result is placed in the accumulator.

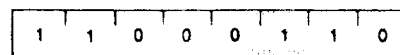


Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

ADI data (Add immediate)

(A) ← (A) + (byte 2)

The content of the second byte of the instruction is added to the content of the accumulator. The result is placed in the accumulator.

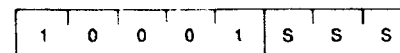


Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

ADC r (Add Register with carry)

(A) ← (A) + (r) + (CY)

The content of register r and the content of the carry bit are added to the content of the accumulator. The result is placed in the accumulator.

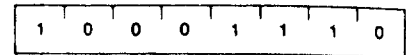


Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ADC M (Add memory with carry)

(A) ← (A) + ((H)(L)) + (CY)

The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are added to the accumulator. The result is placed in the accumulator.

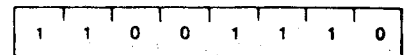


Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

ACI data (Add immediate with carry)

(A) ← (A) + (byte 2) + (CY)

The content of the second byte of the instruction and the content of the CY flag are added to the contents of the accumulator. The result is placed in the accumulator.

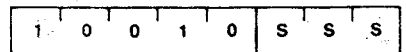


Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

SUB r (Subtract Register)

(A) ← (A) - (r)

The content of register r is subtracted from the content of the accumulator. The result is placed in the accumulator.

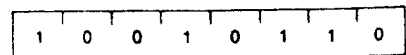


Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

SUB M (Subtract memory)

(A) ← (A) - ((H)(L))

The content of the memory location whose address is contained in the H and L registers is subtracted from the content of the accumulator. The result is placed in the accumulator.

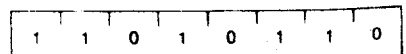


Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

SUI data (Subtract immediate)

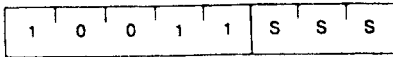
(A) ← (A) - (byte 2)

The content of the second byte of the instruction is subtracted from the content of the accumulator. The result is placed in the accumulator.



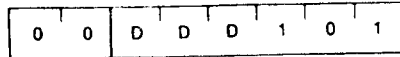
Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

SBB r (Subtract Register with borrow)
 $(A) - (A) - (r) - (CY)$
 The content of register *r* and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.



Cycles: 1
 States: 4
 Addressing: register
 Flags: Z,S,P,CY,AC

DCR r (Decrement Register)
 $(r) - (r) - 1$
 The content of register *r* is decremented by one. Note: All condition flags except CY are affected.

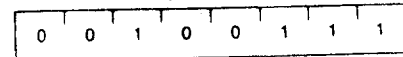


Cycles: 1
 States: 4
 Addressing: register
 Flags: Z,S,P,AC

DAA (Decimal Adjust Accumulator)
 The eight-bit number in the accumulator is adjusted to form two four-bit Binary-Coded-Decimal digits by the following process:

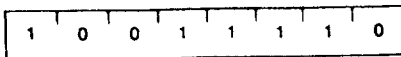
1. If the value of the least significant 4 bits of the accumulator is greater than 9 or if the AC flag is set, 6 is added to the accumulator.
2. If the value of the most significant 4 bits of the accumulator is now greater than 9, or if the CY flag is set, 6 is added to the most significant 4 bits of the accumulator.

NOTE: All flags are affected.



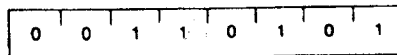
Cycles: 1
 States: 4
 Flags: Z,S,P,CY,AC

SBB M (Subtract memory with borrow)
 $(A) - (A) - ((H)(L)) - (CY)$
 The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.



Cycles: 2
 States: 7
 Addressing: reg. indirect
 Flags: Z,S,P,CY,AC

DCR M (Decrement memory)
 $((H)(L)) - ((H)(L)) - 1$
 The content of the memory location whose address is contained in the H and L registers is decremented by one. Note: All condition flags except CY are affected.



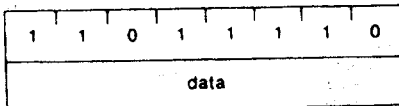
Cycles: 3
 States: 10
 Addressing: reg. indirect
 Flags: Z,S,P,AC

4.6.3 Logic Group

This group of instructions performs logical (Boolean) operations on data in registers and memory and on condition flags.

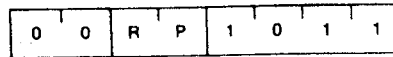
Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Auxiliary Carry, and Carry flags according to the standard rules.

SBI data (Subtract immediate with borrow)
 $(A) - (A) - (\text{byte 2}) - (CY)$
 The contents of the second byte of the instruction and the contents of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.



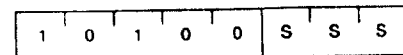
Cycles: 2
 States: 7
 Addressing: immediate
 Flags: Z,S,P,CY,AC

INX rp (Increment register pair)
 $(rh)(rl) - (rh)(rl) + 1$
 The content of the register pair *rp* is incremented by one. Note: No condition flags are affected.



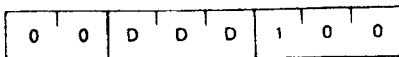
Cycles: 1
 States: 6
 Addressing: register
 Flags: none

ANA r (AND Register)
 $(A) - (A) \wedge (r)$
 The content of register *r* is logically ANDed with the content of the accumulator. The result is placed in the accumulator. The CY flag is cleared and AC is set.



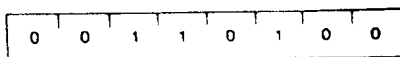
Cycles: 1
 States: 4
 Addressing: register
 Flags: Z,S,P,CY,AC

INR r (Increment Register)
 $(r) - (r) + 1$
 The content of register *r* is incremented by one. Note: All condition flags except CY are affected.



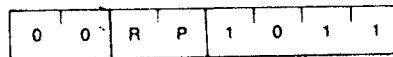
Cycles: 1
 States: 4
 Addressing: register
 Flags: Z,S,P,AC

INR M (Increment memory)
 $((H)(L)) - ((H)(L)) + 1$
 The content of the memory location whose address is contained in the H and L registers is incremented by one. Note: All condition flags except CY are affected.



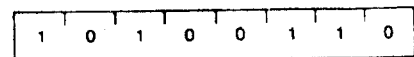
Cycles: 3
 States: 10
 Addressing: reg. indirect
 Flags: Z,S,P,AC

DCX rp (Decrement register pair)
 $(rh)(rl) - (rh)(rl) - 1$
 The content of the register pair *rp* is decremented by one. Note: No condition flags are affected.



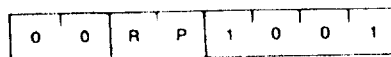
Cycles: 1
 States: 6
 Addressing: register
 Flags: none

ANA M (AND memory)
 $(A) - (A) \wedge ((H)(L))$
 The contents of the memory location whose address is contained in the H and L registers is logically ANDed with the content of the accumulator. The result is placed in the accumulator. The CY flag is cleared and AC is set.



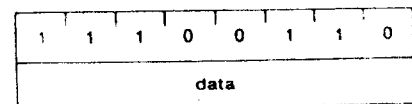
Cycles: 2
 States: 7
 Addressing: reg. indirect
 Flags: Z,S,P,CY,AC

DAD rp (Add register pair to H and L)
 $((H)(L)) - ((H)(L)) + (rh)(rl)$
 The content of the register pair *rp* is added to the content of the register pair H and L. The result is placed in the register pair H and L. Note: Only the CY flag is affected. It is set if there is a carry out of the double precision add, otherwise it is reset.



Cycles: 3
 States: 10
 Addressing: register
 Flags: CY

ANI data (AND immediate)
 $(A) - (A) \wedge (\text{byte 2})$
 The content of the second byte of the instruction is logically ANDed with the contents of the accumulator. The result is placed in the accumulator. The CY flag is cleared and AC is set.

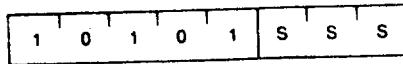


Cycles: 2
 States: 7
 Addressing: immediate
 Flags: Z,S,P,CY,AC

XRA r (Exclusive OR Register)

(A) ← (A) ∨ (r)

The content of register r is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

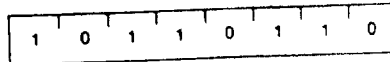


Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ORA M (OR memory)

(A) ← (A) ∨ ((H) (L))

The content of the memory location whose address is contained in the H and L registers is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

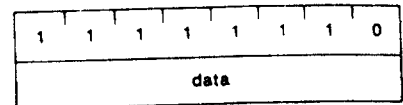


Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

CPI data (Compare immediate)

(A) ← (byte 2)

The content of the second byte of the instruction is subtracted from the accumulator. The condition flags are set by the result of the subtraction. The Z flag is set to 1 if (A) = (byte 2). The CY flag is set to 1 if (A) < (byte 2).

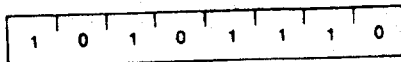


Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

XRA M (Exclusive OR Memory)

(A) ← (A) ∨ ((H) (L))

The content of the memory location whose address is contained in the H and L registers is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

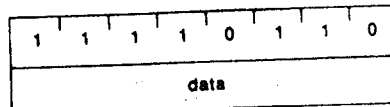


Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

ORI data (OR Immediate)

(A) ← (A) ∨ (byte 2)

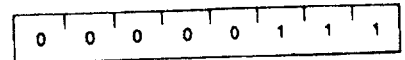
The content of the second byte of the instruction is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.



Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

RLC (Rotate left)(A_{n+1}) ← (A_n); (A₀) ← (A₇)(CY) ← (A₇)

The content of the accumulator is rotated left one position. The low order bit and the CY flag are both set to the value shifted out of the high order bit position. Only the CY flag is affected.

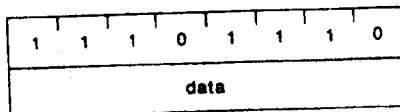


Cycles: 1
States: 4
Flags: CY

XRI data (Exclusive OR immediate)

(A) ← (A) ∨ (byte 2)

The content of the second byte of the instruction is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

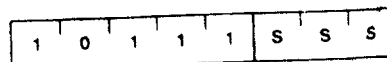


Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

CMP r (Compare Register)

(A) ← (r)

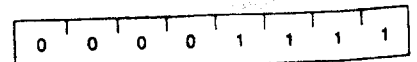
The content of register r is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = (r). The CY flag is set to 1 if (A) < (r).



Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

RRC (Rotate right)(A_n) ← (A_{n+1}); (A₇) ← (A₀)(CY) ← (A₀)

The content of the accumulator is rotated right one position. The high order bit and the CY flag are both set to the value shifted out of the low order bit position. Only the CY flag is affected.

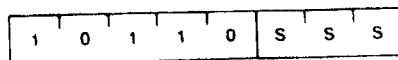


Cycles: 1
States: 4
Flags: CY

ORA r (OR Register)

(A) ← (A) ∨ (r)

The content of register r is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

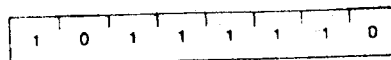


Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

CMP M (Compare memory)

(A) ← ((H) (L))

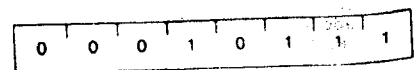
The content of the memory location whose address is contained in the H and L registers is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = ((H) (L)). The CY flag is set to 1 if (A) < ((H) (L)).



Cycles: 2
States: 7
Addressing: reg. indirect
Flags: Z,S,P,CY,AC

RAL (Rotate left through carry)(A_{n+1}) ← (A_n); (CY) ← (A₇)(A₀) ← (CY)

The content of the accumulator is rotated left one position through the CY flag. The low order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high order bit. Only the CY flag is affected.

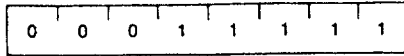


Cycles: 1
States: 4
Flags: CY

RAR (Rotate right through carry)

$(A_n) - (A_{n-1}); (CY) - (A_0)$
 $(A_7) - (CY)$

The content of the accumulator is rotated right one position through the CY flag. The high order bit is set to the CY flag and the CY flag is set to the value shifted out of the low order bit. **Only the CY flag is affected.**

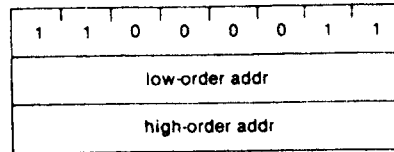


Cycles: 1
 States: 4
 Flags: CY

JMP addr (Jump)

$(PC) - (\text{byte 3})(\text{byte 2})$

Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.



Cycles: 3
 States: 10
 Addressing: immediate
 Flags: none

Ccondition addr (Condition call)

If (CCC),

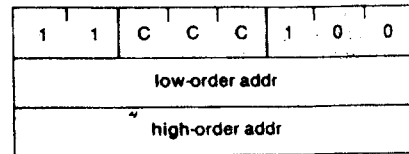
$((SP) - 1) - (PCH)$

$((SP) - 2) - (PCL)$

$(SP) - (SP) - 2$

$(PC) - (\text{byte 3})(\text{byte 2})$

If the specified condition is true, the actions specified in the CALL instruction (see above) are performed; otherwise, control continues sequentially.

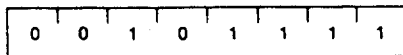


Cycles: 2/5
 States: 9/18
 Addressing: immediate/
 reg. indirect
 Flags: none

CMA (Complement accumulator)

$(A) - (\bar{A})$

The contents of the accumulator are complemented (zero bits become 1, one bits become 0). **No flags are affected.**



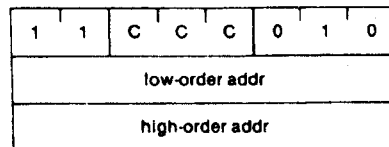
Cycles: 1
 States: 4
 Flags: none

Jcondition addr (Conditional jump)

If (CCC),

$(PC) - (\text{byte 3})(\text{byte 2})$

If the specified condition is true, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction; otherwise, control continues sequentially.



Cycles: 2/3
 States: 7/10
 Addressing: immediate
 Flags: none

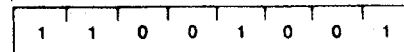
RET (Return)

$(PCL) - ((SP));$

$(PCH) - ((SP) + 1);$

$(SP) - (SP) + 2;$

The content of the memory location whose address is specified in register SP is moved to the low-order eight bits of register PC. The content of the memory location whose address is one more than the content of register SP is moved to the high-order eight bits of register PC. The content of register SP is incremented by 2.

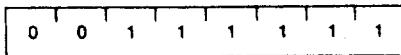


Cycles: 3
 States: 10
 Addressing: reg. indirect
 Flags: none

CMC (Complement carry)

$(CY) - (\bar{CY})$

The CY flag is complemented. **No other flags are affected.**

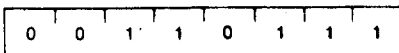


Cycles: 1
 States: 4
 Flags: CY

STC (Set carry)

$(CY) - 1$

The CY flag is set to 1. **No other flags are affected.**



Cycles: 1
 States: 4
 Flags: CY

CALL addr (Call)

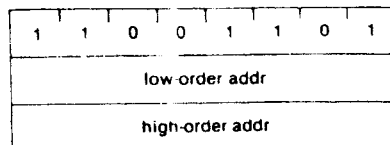
$((SP) - 1) - (PCH)$

$((SP) - 2) - (PCL)$

$(SP) - (SP) - 2$

$(PC) - (\text{byte 3})(\text{byte 2})$

The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.



Cycles: 5
 States: 18
 Addressing: immediate/
 reg. indirect
 Flags: none

Rcondition (Conditional return)

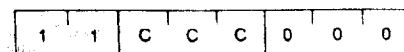
If (CCC),

$(PCL) - ((SP))$

$(PCH) - ((SP) + 1)$

$(SP) - (SP) + 2$

If the specified condition is true, the actions specified in the RET instruction (see above) are performed; otherwise, control continues sequentially.



Cycles: 1/3
 States: 6/12
 Addressing: reg. indirect
 Flags: none

4.6.4 Branch Group

This group of instructions alter normal sequential program flow.

Condition flags are not affected by any instruction in this group.

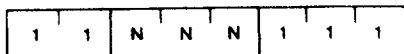
The two types of branch instructions are unconditional and conditional. Unconditional transfers simply perform the specified operation on register PC (the program counter). Conditional transfers examine the status of one of the four processor flags to determine if the specified branch is to be executed. The conditions that may be specified are as follows:

CONDITION	CCC
NZ — not zero ($Z = 0$)	000
Z — zero ($Z = 1$)	001
NC — no carry ($CY = 0$)	010
C — carry ($CY = 1$)	011
PO — parity odd ($P = 0$)	100
PE — parity even ($P = 1$)	101
P — plus ($S = 0$)	110
M — minus ($S = 1$)	111

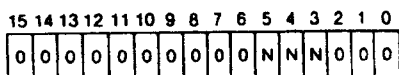
RST n (Restart)

$((SP) - 1) - (PCH)$
 $((SP) - 2) - (PCL)$
 $(SP) - (SP) - 2$
 $(PC) - 8 * (NNN)$

The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two. Control is transferred to the instruction whose address is eight times the content of NNN.



Cycles: 3
 States: 12
 Addressing: reg. indirect
 Flags: none

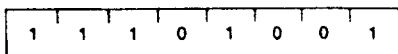


Program Counter After Restart

PCHL (Jump H and L indirect — move H and L to PC)

$(PCH) - (H)$
 $(PCL) - (L)$

The content of register H is moved to the high-order eight bits of register PC. The content of register L is moved to the low-order eight bits of register PC.



Cycles: 1
 States: 6
 Addressing: register
 Flags: none

4.6.5 Stack, I/O, and Machine Control Group

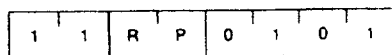
This group of instructions performs I/O, manipulates the Stack, and alters internal control flags.

Unless otherwise specified, condition flags are not affected by any instructions in this group.

PUSH rp (Push)

$((SP) - 1) - (rh)$
 $((SP) - 2) - (rl)$
 $((SP) - (SP) - 2$

The content of the high-order register of register pair *rp* is moved to the memory location whose address is one less than the content of register SP. The content of the low-order register of register pair *rp* is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Note: Register pair *rp* = SP may not be specified.

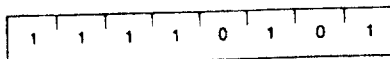


Cycles: 3
 States: 12
 Addressing: reg. indirect
 Flags: none

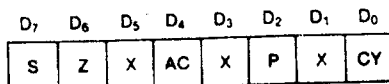
PUSH PSW (Push processor status word)

$((SP) - 1) - (A)$
 $((SP) - 2)_0 - (CY), ((SP) - 2)_1 - X$
 $((SP) - 2)_2 - (P), ((SP) - 2)_3 - X$
 $((SP) - 2)_4 - (AC), ((SP) - 2)_5 - X$
 $((SP) - 2)_6 - (Z), ((SP) - 2)_7 - (S)$
 $((SP) - (SP) - 2$ X: Undefined.

The content of register A is moved to the memory location whose address is one less than register SP. The contents of the condition flags are assembled into a processor status word and the word is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two.



Cycles: 3
 States: 12
 Addressing: reg. indirect
 Flags: none

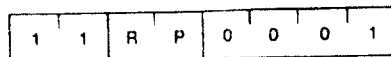
FLAG WORD

X: undefined

POP rp (POP)

$(rl) - ((SP))$
 $(rh) - ((SP) + 1)$
 $(SP) - (SP) + 2$

The content of the memory location, whose address is specified by the content of register SP, is moved to the low-order register of register pair *rp*. The content of the memory location, whose address is one more than the content of register SP, is moved to the high-order register of register pair *rp*. The content of register SP is incremented by 2. Note: Register pair *rp* = SP may not be specified.

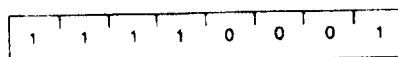


Cycles: 3
 States: 10
 Addressing: reg. indirect
 Flags: none

POP PSW (Pop processor status word)

$(CY) - ((SP))_0$
 $(P) - ((SP))_2$
 $(AC) - ((SP))_4$
 $(Z) - ((SP))_6$
 $(S) - ((SP))_7$
 $(A) - ((SP) + 1)$
 $(SP) - (SP) + 2$

The content of the memory location whose address is specified by the content of register SP is used to restore the condition flags. The content of the memory location whose address is one more than the content of register SP is moved to register A. The content of register SP is incremented by 2.

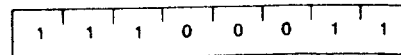


Cycles: 3
 States: 10
 Addressing: reg. indirect
 Flags: Z,S,P,CY,AC

XTHL (Exchange stack top with H and L)

$(L) - ((SP))$
 $(H) - ((SP) + 1)$

The content of the L register is exchanged with the content of the memory location whose address is specified by the content of register SP. The content of the H register is exchanged with the content of the memory location whose address is one more than the content of register SP.

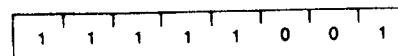


Cycles: 5
 States: 16
 Addressing: reg. indirect
 Flags: none

SPHL (Move HL to SP)

$(SP) - (H) (L)$

The contents of registers H and L (16 bits) are moved to register SP.

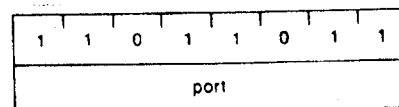


Cycles: 1
 States: 6
 Addressing: register
 Flags: none

IN port (Input)

$(A) - (data)$

The data placed on the eight bit bi-directional data bus by the specified port is moved to register A.

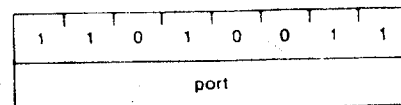


Cycles: 3
 States: 10
 Addressing: direct
 Flags: none

OUT port (Output)

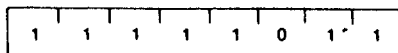
$(data) - (A)$

The content of register A is placed on the eight bit bi-directional data bus for transmission to the specified port.



Cycles: 3
 States: 10
 Addressing: direct
 Flags: none

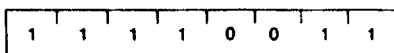
EI (Enable interrupts)
The interrupt system is enabled following the execution of the next instruction.



Cycles: 1
States: 4
Flags: none

NOTE: Interrupts are not recognized during the EI instruction. Placing an EI instruction on the bus in response to INTA during an INA cycle is prohibited.

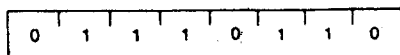
DI (Disable interrupts)
The interrupt system is disabled immediately following the execution of the DI instruction.



Cycles: 1
States: 4
Flags: none

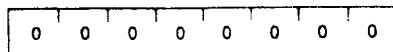
NOTE: Interrupts are not recognized during the DI instruction. Placing a DI instruction on the bus in response to INTA during an INA cycle is prohibited.

HLT (Halt)
The processor is stopped. The registers and flags are unaffected. A second ALE is generated during the execution of HLT to strobe out the Halt cycle status information.



Cycles: 1+
States: 5
Flags: none

NOP (No op)
No operation is performed. The registers and flags are unaffected.

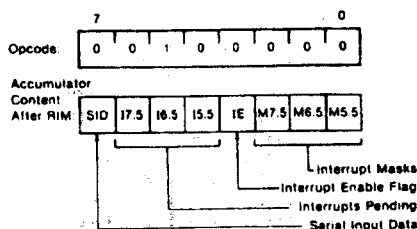


Cycles: 1
States: 4
Flags: none

RIM (Read Interrupt Masks)
The RIM instruction loads data into the accumulator relating to interrupts and the serial input. This data contains the following information:

- Current interrupt mask status for the RST 5.5, 6.5, and 7.5 hardware interrupts (1 = mask disabled)
- Current interrupt enable flag status (1 = interrupts enabled) except immediately following a TRAP interrupt. (See below.)
- Hardware interrupts pending (i.e., signal received but not yet serviced), on the RST 5.5, 6.5, and 7.5 lines.
- Serial input data.

Immediately following a TRAP interrupt, the RIM instruction must be executed as a part of the service routine if you need to retrieve current interrupt status later. Bit 3 of the accumulator is (in this special case only) loaded with the interrupt enable (IE) flag status that existed prior to the TRAP interrupt. Following an RST 5.5, 6.5, 7.5, or INTR interrupt, the interrupt flag flip-flop reflects the current interrupt enable status. Bit 6 of the accumulator (I7.5) is loaded with the status of the RST 7.5 flip-flop, which is always set (edge-triggered) by an input on the RST 7.5 input line, even when that interrupt has been previously masked. (See SIM instruction.)



Cycles: 1
States: 4
Flags: none

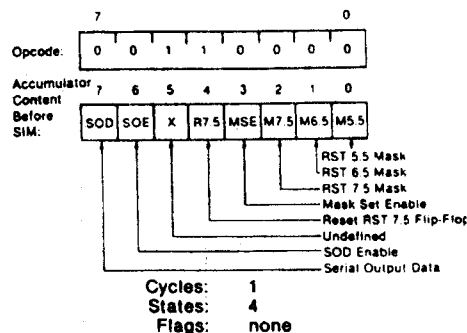
SIM (Set Interrupt Masks)

The execution of the SIM instruction uses the contents of the accumulator (which must be previously loaded) to perform the following functions:

- Program the interrupt mask for the RST 5.5, 6.5, and 7.5 hardware interrupts.
- Reset the edge-triggered RST 7.5 input latch.
- Load the SOD output latch.

To program the interrupt masks, first set accumulator bit 3 to 1 and set to 1 any bits 0, 1, and 2, which disable interrupts RST 5.5, 6.5, and 7.5, respectively. Then do a SIM instruction. If accumulator bit 3 is 0 when the SIM instruction is executed, the interrupt mask register will not change. If accumulator bit 4 is 1 when the SIM instruction is executed, the RST 7.5 latch is then reset. RST 7.5 is distinguished by the fact that its latch is always set by a rising edge on the RST 7.5 input pin, even if the jump to service routine is inhibited by masking. This latch remains high until cleared by a RESET IN, by a SIM instruction with accumulator bit 4 high, or by an internal processor acknowledge to an RST 7.5 interrupt subsequent to the removal of the mask (by a SIM instruction). The RESET IN signal always sets all three RST mask bits.

If accumulator bit 6 is at the 1 level when the SIM instruction is executed, the state of accumulator bit 7 is loaded into the SOD latch and thus becomes available for interface to an external device. The SOD latch is unaffected by the SIM instruction if bit 6 is 0. SOD is always reset by the RESET IN signal.



Cycles: 1
States: 4
Flags: none

ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED

Adr = 16-bit address

ASCII Code Table

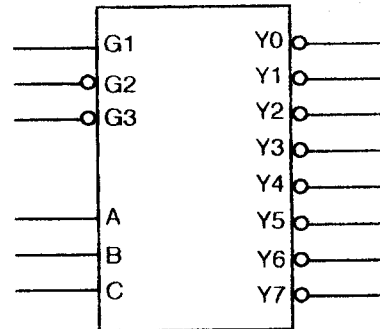
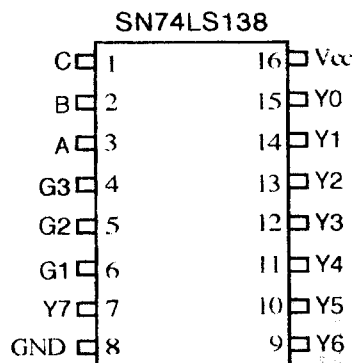
DECIMAL VALUE	HEX DECIMAL VALUE	0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240
0	0	BLANK (NULL)	▶	BLANK (SPACE)	0	@	P	'	p	Ç	É	á	1/4 Del	1/2 Del	3/4 Del	∞	≡
1	1	☺	◀	!	1	A	Q	a	q	ü	Æ	ï	1/4 Del	1/2 Del	3/4 Del	β	±
2	2	☹	↑	"	2	B	R	b	r	é	FE	ó	1/4 Del	1/2 Del	3/4 Del	γ	≥
3	3	♥	!!	#	3	C	S	c	s	â	ô	ú	1/4 Del	1/2 Del	3/4 Del	π	≤
4	4	♦	¶	\$	4	D	T	d	t	ä	ö	ñ	1/4 Del	1/2 Del	3/4 Del	Σ	∫
5	5	♣	§	%	5	E	U	e	u	à	ò	Ñ	1/4 Del	1/2 Del	3/4 Del	σ	∫
6	6	♠	—	&	6	F	V	f	v	â	û	ä	1/4 Del	1/2 Del	3/4 Del	μ	÷
7	7	•	↓	'	7	G	W	g	w	Ç	ù	o	1/4 Del	1/2 Del	3/4 Del	τ	≈
8	8	•	↑	(8	H	X	h	x	ê	ÿ	ı	1/4 Del	1/2 Del	3/4 Del	Φ	°
9	9	○	↓)	9	I	Y	i	y	ë	Ö	┐	1/4 Del	1/2 Del	3/4 Del	Θ	•
10	A	○	→	*	:	J	Z	j	x	è	Ü	┐	1/4 Del	1/2 Del	3/4 Del	Ω	•
11	B	♂	←	+	;	K	I	k	{	ï	ç	½	1/4 Del	1/2 Del	3/4 Del	δ	√
12	C	♀	└	,	<	L	\	l		î	£	¼	1/4 Del	1/2 Del	3/4 Del	∞	η
13	D	♪	↔	—	=	M	I	m	}	ì	¥	ı	1/4 Del	1/2 Del	3/4 Del	∅	²
14	E	♪	▲	.	>	N	^	n	~	À	Pts	«	1/4 Del	1/2 Del	3/4 Del	€	■
15	F	☼	▼	/	?	O	_	o	Δ	Ä	f	»	1/4 Del	1/2 Del	3/4 Del	∩	BLANK FF

[illegible]

[illegible]

Pengkodan SN74LS138

Rajah pin keluaran dan simbolnya



Jadual fungsi

G1	G2	G3	A	B	C		Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	1	X	X	X		1	1	1	1	1	1	1	1
X	1	X	X	X	X		1	1	1	1	1	1	1	1
0	X	X	X	X	X		1	1	1	1	1	1	1	1
1	0	0	0	0	0		0	1	1	1	1	1	1	1
1	0	0	0	0	1		1	0	1	1	1	1	1	1
1	0	0	0	1	0		1	1	0	1	1	1	1	1
1	0	0	0	1	1		1	1	1	0	1	1	1	1
1	0	0	1	0	0		1	1	1	1	0	1	1	1
1	0	0	1	0	1		1	1	1	1	1	0	1	1
1	0	0	1	1	0		1	1	1	1	1	1	0	1
1	0	0	1	1	1		1	1	1	1	1	1	1	0

8085AH/8085AH-2/8085AH-1 8-BIT HMOS MICROPROCESSORS

- Single +5V Power Supply with 10% Voltage Margins
- 3 MHz, 5 MHz and 6 MHz Selections Available
- 20% Lower Power Consumption than 8085A for 3 MHz and 5 MHz
- 1.3 μ s Instruction Cycle (8085AH); 0.8 μ s (8085AH-2); 0.67 μ s (8085AH-1)
- 100% Software Compatible with 8080A
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is Non-Maskable) Plus an 8080A-Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory
- Available in 40-Lead Cerdip and Plastic Packages (See Packaging Spec, Order #231369)

The Intel 8085AH is a complete 8 bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's (8085AH (CPU), 8156H (RAM/IO) and 8755A (EPROM/IO)) while maintaining total system expandability. The 8085AH-2 and 8085AH-1 are faster versions of the 8085 AH.

The 8085AH incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a higher level of system integration.

The 8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155H/8156H/8755A memory products allow a direct interface with the 8085AH.

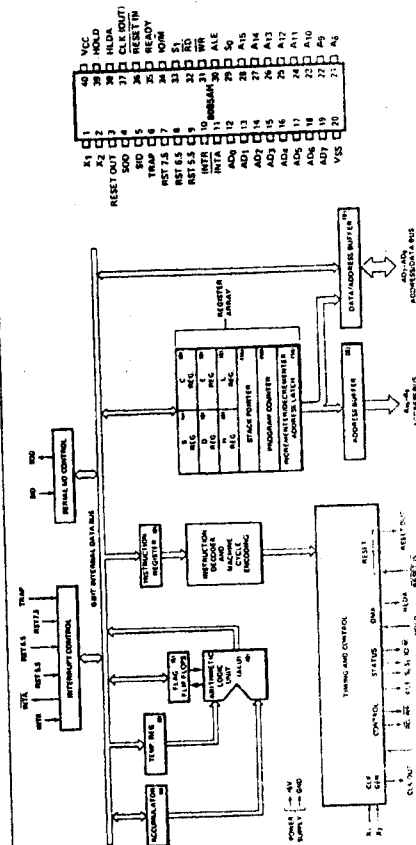


Figure 1. 8085AH CPU Functional Block Diagram

Figure 2. 8085AH Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function	Symbol	Type	Name and Function
A ₀ -A ₁₅	O	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address. 3-stated during Hold and Halt modes and during RESET.	READY	I	Ready: If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
AD ₀ -7	I/O	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T ₁ state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.	HOLD	I	Hold: Indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, RD, WR, and I/O M lines are 3-stated.
ALE	O	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.	HLDA	O	Hold Acknowledge: Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the HOLD request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.
SP, S ₁ , and I/O M	O	Machine Cycle Status: I/O M S ₁ S ₀ Status 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode latch 1 1 1 Interrupt • 0 0 Halt • X X Hold • X X Reset • = 3-state (high impedance) X = unspecified	INTR	I	Interrupt Request: Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESET or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
RD	O	Read Control: A low level on RD indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. 3-stated during Hold and Halt modes and during RESET.	INTA	O	Interrupt Acknowledge: Is used instead of (and has the same timing as) RD during the instruction cycle after an INTR is accepted. It can be used to activate an 8259A interrupt chip or some other interrupt port.
WR	O	Write Control: A low level on WR indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3-stated during Hold and Halt modes and during RESET.	RST 5.5 RST 6.5 RST 7.5	I	Restart Interrupts: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
TRAP	I	Trap: Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5. It is unaffected by any mask or interrupt enable. It has the highest priority of any interrupt. (See Table 2.)
RESET IN	I	Reset In: Sets the Program Counter to zero and resets the interrupt enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET. Because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 3). Upon power-up, RESET IN must remain low for at least 10 ms after minimum V _{CC} has been reached. For proper reset operation after the power-up duration, RESET IN should be kept low a minimum of three clock periods. The CPU shield in the reset condition as long as RESET IN is applied.

Symbol	Type	Name and Function
RESET OUT	O	Reset Out: Reset Out indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X ₁ , X ₂	I	X ₁ and X ₂ : Are connected to a crystal, LC, or RC network to drive the internal clock generator. X ₁ can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK	O	Clock: Clock output for use as a system clock. The period of CLK is twice the X ₁ , X ₂ input period.
SIO	I	Serial Input Data Line: The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	O	Serial Output Data Line: The output SOD is set or reset as specified by the SIM instruction.
V _{CC}		Power: +5 volt supply.
V _{SS}		Ground: Reference.

Table 2. Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1)	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.

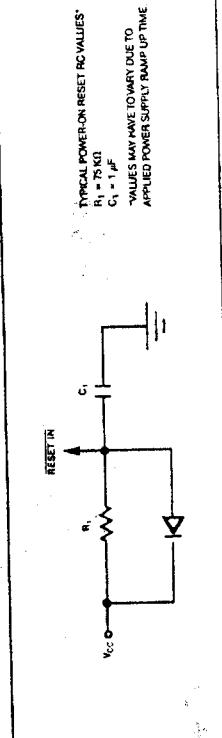


Figure 3. Power-On Reset Circuit

FUNCTIONAL DESCRIPTION

The 8085AH is a complete 8-bit parallel central processor. It is designed with N-channel, depletion load, silicon gate technology (HMOS), and requires a single +5-volt supply. Its basic clock speed is 3 MHz (8085AH), 5 MHz (8085AH-2), or 6 MHz (8085AH-1), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (8085AH), a RAM/IO (8156H), and an EPROM/IO chip (8755A).

The 8085AH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085AH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers: data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 8085AH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085AH provides RD, WR, S₀, S₁, and I/O/M signals for bus control. An interrupt acknowledge signal (INTA) is also provided. HOLD and all interrupts are synchronized with the processor's internal clock. The 8085AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085AH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt, and a bus vectored interrupt, INTR.

INTERRUPT AND SERIAL I/O

The 8085AH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs (5.5, 6.5, and 7.5) has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 2.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive*.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request (a normally high level signal with a low going pulse is recommended for highest system noise immunity). The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 8085AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN. (See SIM, Chapter 5 of the 8080/8085 User's Manual.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP—highest priority, RST 7.5, RST 6.5, RST 5.5, INTR—lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

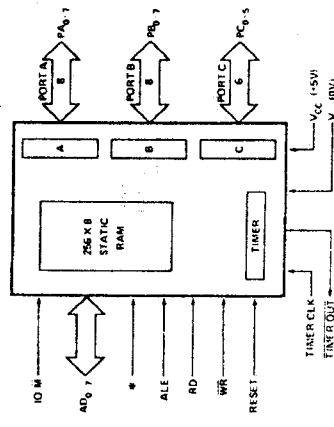
The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive*. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 4 illustrates the TRAP interrupt request circuitry within the 8085AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

8155H/8156H/8155H-2/8156H-2 2048-BIT STATIC HMOS RAM WITH I/O PORTS AND TIMER

- Single +5V Power Supply with 10% Voltage Margins
- 30% Lower Power Consumption than the 8155 and 8156
- 256 Word x 8 Bits
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8-Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with 8085AH and 8088 CPU
- Multiplexed Address and Data Bus
- Available in EXPRESS
- Standard Temperature Range
- Extended Temperature Range

The Intel® 8155H and 8156H are RAM and I/O chips implemented in N-Channel, depletion load, silicon gate technology (HMOS), to be used in the 8085AH and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085AH CPU. The 8155H-2 and 8156H-2 have maximum access times of 330 ns for use with the 8085AH-2 and the 5 MHz 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode. A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.



*8155H/8156H-2 = CE, 8156H/8156H-2 = CE

Figure 1. Block Diagram

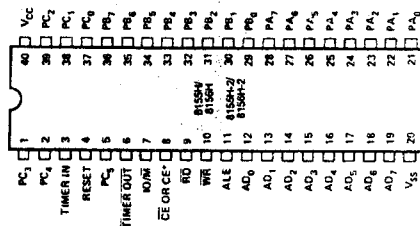


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
RESET	I	Reset: Pulse provided by the 8085AH to initialize the system (connect to 8085AH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085AH clock cycle times.
AD ₀₋₇	I/O	Address/Data: 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched inside the 8155H/8156H on the falling edge of ALE. The 8-bit data is either written into the chip or read from the chip, depending on the WR or RD input signal.
CE or \overline{CE}	I	Chip Enable: On the 8155H, this pin is \overline{CE} and is ACTIVE LOW. On the 8156H, this pin is CE and is ACTIVE HIGH.
\overline{RD}	I	Read Control: Input low on this line with the Chip Enable active enables and AD ₀₋₇ buffers. If IO/M pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
\overline{WR}	I	Write Control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status registers, depending on IO/M.
ALE	I	Address Latch Enable: This control signal latches both the address on the AD ₀₋₇ lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.
IO/M	I	I/O Memory: Selects memory if low and I/O and command/status registers if high.
PA ₀₋₇ (8)	I/O	Port A: These 8 pins are general purpose I/O pins. The input direction is selected by programming the command register.
PB ₀₋₇ (8)	I/O	Port B: These 8 pins are general purpose I/O pins. The input direction is selected by programming the command register.
PC ₀₋₅ (6)	I/O	Port C: These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC ₀₋₅ are used as control signals, they will provide the following: PC ₀ — A INTR (Port A Interrupt) PC ₁ — ABF (Port A Buffer Full) PC ₂ — A STB (Port A Strobe) PC ₃ — B INTR (Port B Interrupt) PC ₄ — B BF (Port B Buffer Full) PC ₅ — B STB (Port B Strobe)
TIMER IN	I	Timer Input: Input to the counter-timer.
TIMER OUT	O	Timer Output: The output can be either a square wave or a pulse, depending on the timer mode.
V _{CC}		Voltage: +5 volt supply.
V _{SS}		Ground: Ground reference.

FUNCTIONAL DESCRIPTION

The 8155H/8156H contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/M (I/O/Memory Select) pin selects either the five registers (Command, Status, PA₀₋₇, PB₀₋₇, PC₀₋₅) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines. Chip Enable input CE or \overline{CE} , and IO/M are all latched on-chip at the falling edge of ALE.

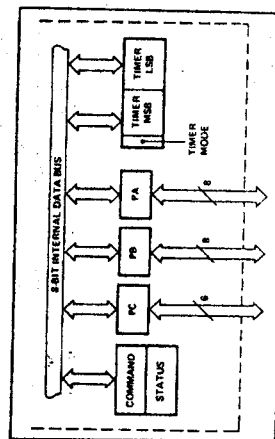


Figure 3. 8155H/8156H Internal Registers

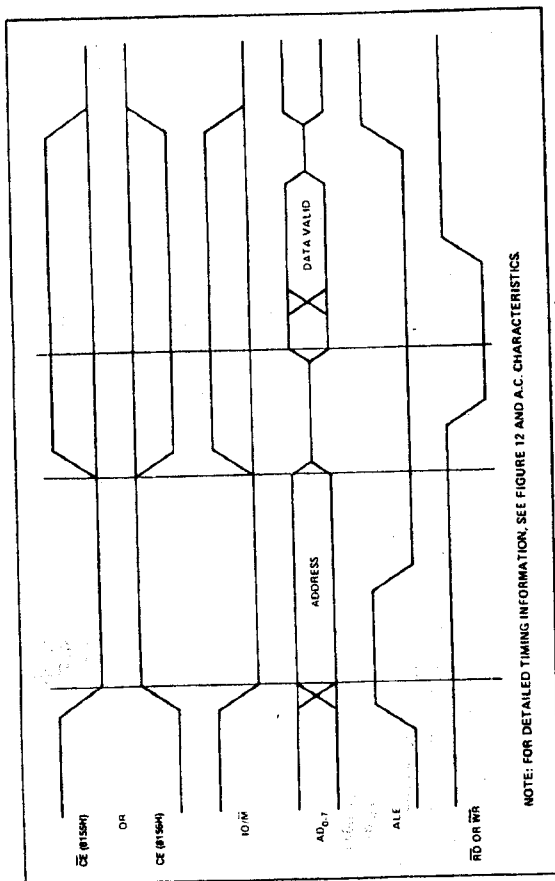


Figure 4. 8155H/8156H On-Board Memory Read/Write Cycle

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports. Two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer. The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and $\text{IO}/\text{M} = 1$. The meaning of each bit of the command byte is defined in Figure 5. The contents of the command register may never be read.

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit: six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 6. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

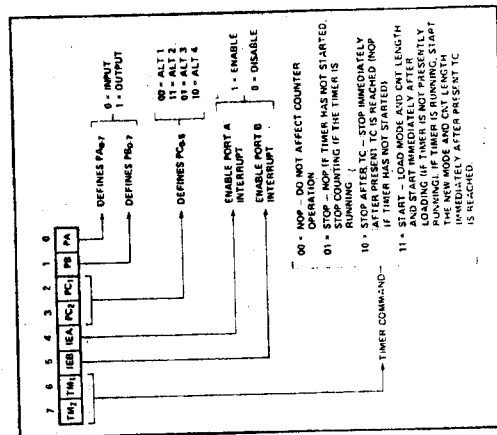


Figure 5. Command Register Bit Assignment

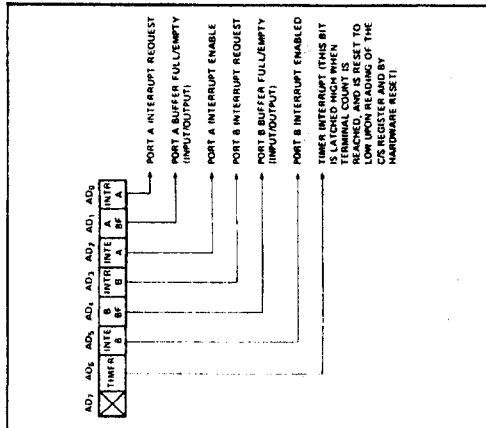


Figure 6. Status Register Bit Assignment

INPUT/OUTPUT SECTION

The I/O section of the 8155H/8156H consists of five registers. (See Figure 7.)

- **Command/Status Register (C/S)** — Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose. When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are not accessible through the pins.
- **PA Register** — This register has the address XXXXX001 and contains information of the I/O ports and the timer becomes available on the AD₀₋₇ lines.
- **PB Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA₀₋₇. The address of this register is XXXXX001.
- **PC Register** — This register functions the same as PA Register. The I/O pins assigned are PB₀₋₇. The address of this register is XXXXX010.
- **PD Register** — This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD₂ and AD₃ bits of the C/S register.

When PC₀₋₅ is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an

interrupt that the 8155H sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode (See Table 2).

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS ¹								SELECTION	
A7	A6	A5	A4	A3	A2	A1	A0	Interval Command Status Register	General Purpose I/O Port A
X	X	X	X	X	0	0	0	Interval Command Status Register	General Purpose I/O Port A
X	X	X	X	X	0	0	1	General Purpose I/O Port B	General Purpose I/O Port B
X	X	X	X	X	1	0	0	Port C — General Purpose Count	Port C — General Purpose Count
X	X	X	X	X	1	0	1	High 8 bits of Timer Count	High 8 bits of Timer Count
X	X	X	X	X	1	1	0	High 8 bits of Timer Count and 2 bits of Timer Mode	High 8 bits of Timer Count and 2 bits of Timer Mode
X	X	X	X	X	1	1	1	of Timer Mode	of Timer Mode

X: Don't Care.
¹ I/O Address must be qualified by CE = 1 (8156H) or CE = 0 (8155H) and $\text{IO}/\text{M} = 1$ in order to select the appropriate register.

Figure 7. I/O Port and Timer Addressing Scheme

Figure 8 shows how I/O PORTS A and B are structured within the 8155H and 8156H:

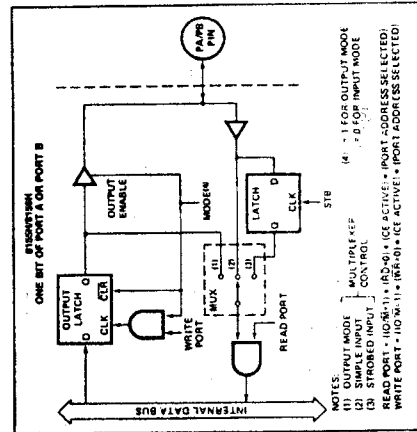


Figure 8. 8155H/8156H Port Functions

Table 2. Port Control Assignment

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A STB (Port A Strobe)	A STB (Port A Strobe)
PC3	Input Port	Output Port	B INTR (Port B Interrupt)	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	B BF (Port B Buffer Full)	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	B STB (Port B Strobe)	B STB (Port B Strobe)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the 8155H/8156H are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the 8155H/8156H is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 9 shows how the 8155H/8156H I/O ports might be configured in a typical MCS-85 system.

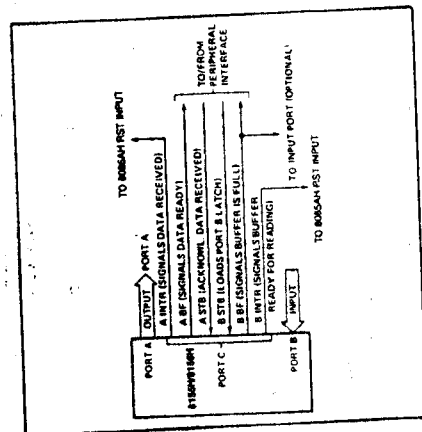


Figure 9. Example: Command Register = 00111001

TIMER SECTION

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 10).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 10). The value loaded into the count length register can have any value from 2H through 3FFFH in Bits 0-13.

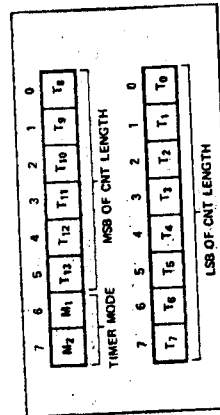


Figure 10. Timer Format

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 11.

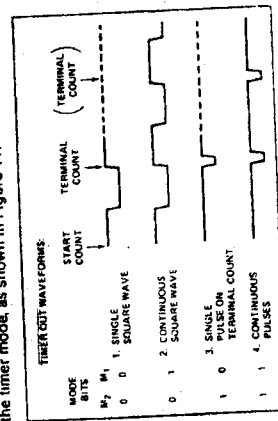


Figure 11. Timer Modes

Bits 6-7, TM2, and TM1 of command register contents are used to start and stop the counter. There are four commands to choose from:

TM2	TM1
0	0
0	1
1	0
1	1

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 12.

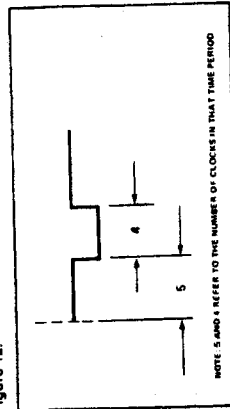


Figure 12. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the 8155H is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the 8155H/8156H chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by two's twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085AH be used. After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count - 1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the 8155H/8156H always counts out the right number of pulses in generating the TIMER OUT waveforms.

8755A/8755A-2 16,384-BIT EPROM WITH I/O

- 2048 Words x 8 Bits
- Single +5V Power Supply (V_{CC})
- Directly Compatible with 8085A and 8088 Microprocessors
- U.V. Erasable and Electrically Reprogrammable
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40-Pin DIP
- Available in EXPRESS
- Standard Temperature Range
- Extended Temperature Range

The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the 8085AH and IAPX 88 microprocessor systems. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085AH CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

The 8755A-2 is a high speed selected version of the 8755A compatible with the 5 MHz 8085AH-2 and the 5 MHz IAPX 88 microprocessor.

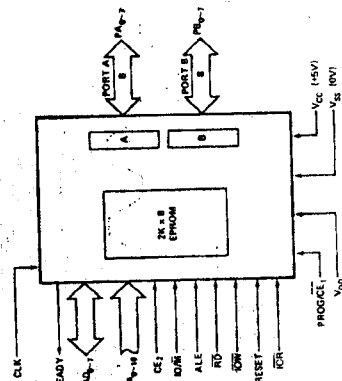


Figure 1. Block Diagram

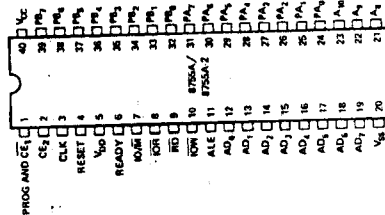


Figure 2. Pin Configuration

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Table 1. Pin Description

Symbol	Type	Name and Function	Symbol	Type	Name and Function
ALE	1	Address Latch Enable: When Address Latch Enable goes high, AD_0-7 , $I/O/M$, A_8-10 , CE_2 , and CE_1 enter the address latches. The signals AD_0 , $I/O/M$, AD_8-10 , CE_2 , CE_1 are latched in at the trailing edge of ALE.	READY	0	Ready is a 3-state output controlled by CE_1 , CE_2 , ALE and CLK. READY is low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK. (See Figure 5c.)
AD_0-7	1	Bidirectional Address/Data Bus: The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B is selected based on the latched value of AD_0 . If RD or IOR is low when the latched Chip Enables are active, the output buffers present data on the bus.	PA_0-7	I/O	Port A: These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and IOW is low and a 0 was previously latched from AD_0 , AD_1 . Read Operation is selected by either IOR low and active Chip Enables and AD_0 and AD_1 low, or IOM high, RD low, active Chip Enables, and AD_0 and AD_1 low.
A_8-10	1	Address Bus: These are the high order bits of the PROM address. They do not affect I/O operations.	PB_0-7	I/O	Port B: This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0 and a 0 from AD_1 .
$PROG/CE_1$ CE_2	1	Chip Enable Inputs: CE_1 is active low and CE_2 is active high. The 8755A can be accessed only when both Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_0-7 and READY outputs will be in a high impedance state. CE_1 is also used as a programming pin. (See section on programming.)	RESET	1	Reset: In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$I/O/M$	1	I/O Memory: If the latched $I/O/M$ is high when RD is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.	IOR	1	I/O Read: When the Chip Enables are active, a low on IOR will output the selected I/O port onto the AD bus. IOR low performs the same function as the combination of IOM high and RD low. When IOR is not used in a system, IOR should be tied to V_{CC} ("1").
RD	1	Read: If the latched Chip Enables are active when RD goes low, the AD_0-7 output buffers are enabled and output either the selected PROM location or I/O port. When both RD and IOR are high, the AD_0-7 output buffers are 3-stated.	V_{CC}		Power: +5 volt supply.
IOW	1	I/O Write: If the latched Chip Enables are active, a low on IOW causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_0-7 . The state of IOM is ignored.	V_{SS}		Ground: Reference.
CLK	1	Clock: The CLK is used to force the READY into its high impedance state after it has been forced low by CE_1 low, CE_2 high, and ALE high.	V_{DD}		Power Supply: V_{DD} is a programming voltage, and must be tied to V_{CC} when the 8755A is being read. For programming, a high voltage is supplied with $V_{DD} = 25V$, typical. (See section on programming.)

System Interface with 8085AH and iAPX 88

A system using the 8755A can use either one of the two I/O interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE₂ and CE₁. By using a combination of unused address lines A₁₁–15 and the Chip Enable inputs, the 8085AH system can use up to 5 each 47555A's without requiring a CE decoder. See Figure 4a and 4b.

If a memory mapped I/O approach is used the 8755A will be selected by the combination of both the $\overline{\text{Chip}}$ Enable and $\overline{\text{IO/M}}$ using AD_{8--15} address lines. See Figure 3.

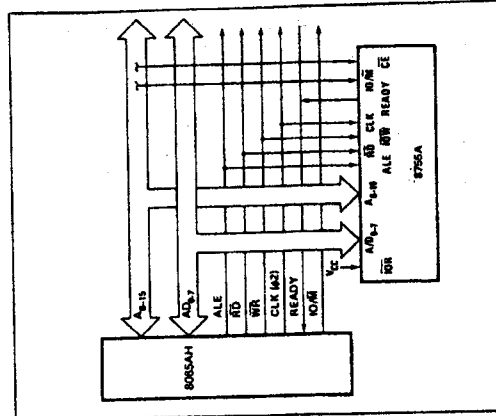


Figure 3. 8755A in 8085AH System (Memory-Mapped I/O)

ERASURE CHARACTERISTICS

The erasure characteristics of the 8755A are such that the erasure process begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (4000 Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8755A in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755 window to prevent unintentional erasure.

The recommended erasure procedure for the 8755A is a 10-minute exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose (i.e. the product of UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000W/cm² power rating. The 8755A should be placed within one inch from the lamp during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

PROGRAMMING

Initially, and after each erasure, all bits of the EPROM portions of the 8755A are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 8755A can be programmed on the Intel® Universal PROM Programmer (UPOP), and the PROMPT™ 80/85 and PROMPT-48™ design aids. The appropriate programming modules and adapters for use in programming both 8755A's and 8755's are shown in Table 1.

The program mode itself consists of programming a single address at a time, giving a single 50 msec pulse for every address. Generally, it is desirable to have a verify cycle after a program cycle for the same address as shown in the attached timing diagram. In the verify cycle (i.e., normal memory read cycle) V_{DD} should be at +5V.

Preliminary timing diagrams and parameter values pertaining to the 8755A programming operation are contained in Figure 7.

intel

FUNCTIONAL DESCRIPTION

PROM Section

PROM Section

The PROM section of the chip is addressed by the 11-bit address and the Chip Enables. The addresses, CE₁, and CE₂ are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and the I/O/M is low when RD goes low, the contents of the PROM location addressed by the latched address are put out on the AD₀₋₇ lines (provided that V_{DD} is tied to V_{CC}.)

I/O Section

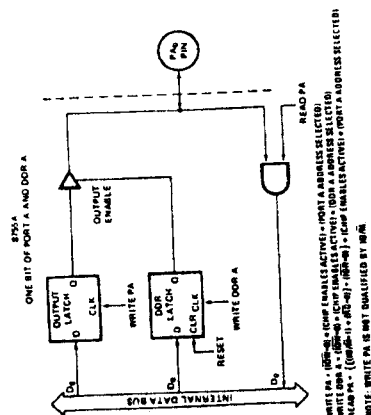
I/O section The I/O section of the chip is addressed by the latched value of AD₀₋₁. Two 8-bit Data Direction Registers (DDR) in 8755A determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position in a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the 8755A are bit-programmable as inputs or outputs. The table summarizes port and DDR designation. DDR1 cannot be read.

Selection	
AD1	AD0
0	0
0	1
1	0
1	1

When **IOW** goes low and the Chip Enables are active, the data on the **AD₀₋₇** is written into I/O port selected by the latched value of **AD₀₋₁**. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of **IOM**. The actual output level does not change until **IOW** returns high. (glitch free output)

A port can be read out when the latched Chip Enables are active and either RD goes low with IO/M high, or IOR goes low. Both input and output mode bits of a selected port will appear on lines AD0-7.

To clarify the function of the I/O Ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.



Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the Output Latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized to a known state without enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

TABLE 1. 875SA PROGRAMMING MODULE CROSS REFERENCE

REFERENCE	MODULE NAME	USE WITH
	UPP 855	UPPI(4)
	UPP UP2(2)	UPP 855
	PROMPT 975	PROMPT 80/85(3)
	PROMPT 475	PROMPT 48(1)
	NOTES:	
		1. Described on p. 13-34 of 1978 Data Catalog.
		2. Special adaptor socket.
		3. Described on p. 13-39 of 1978 Data Catalog.
		4. Described on p. 13-77 of 1978 Data Catalog.